APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,137	09/30/2003	Frank E. LeClerg	884.A46US1	6409

21186   7590   06/13/2007
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER
KERVEROS, JAMES C

ART UNIT	PAPER NUMBER
2117	

MAIL DATE	DELIVERY MODE
06/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/676,137	LECLERG ET AL.
	Examiner	Art Unit	
	JAMES C. KERVEROS	2117	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>24 April 2007</u>.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-25</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>1-25</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on <u>09/30/2003</u> is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Claims 1-25, Group I, in the reply filed on

4/24/2007 is acknowledged. Claims 26-50 are withdrawn from further consideration

pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no

allowable generic or linking claim.

This is a non-Final Office Action in response to the present US Application

10/676137, filed: 9/30/2003. Claims 1-25 are presently under examination and pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under
section 122(b), by another filed in the United States before the invention by the
applicant for patent or (2) a patent granted on an application for patent by
another filed in the United States before the invention by the applicant for patent,
except that an international application filed under the treaty defined in section
351(a) shall have the effects for purposes of this subsection of an application
filed in the United States only if the international application designated the
United States and was published under Article 21(2) of such treaty in the English
language.

Claims 1-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Moyes

et al. (US 7,065,688) filed: 2/19/2003.

Regarding independent Claims 1, 5, 8, 12, 16, 21, Moyes discloses a method for

simultaneous multiprocessor memory testing and initialization during system boot, as

illustrated by the flow diagram of Fig. 5, for optimized memory testing and initialization, comprising:

Performing a memory access procedure (step 502) by initializing system links such that each processing node can communicate to other processing nodes and memory, performed by BIOS running on the bootstrap processor (BSP), which causes the memory initialization process to begin (step 504). The BSP can send a start message to each processing node or a broadcast message to all processing nodes. Alternatively, a bit can be written in each processing node indicating the memory initialization and testing process is to begin.

Each processing node performs memory initialization and testing for a portion of memory, step 506, as also illustrated in Fig. 2, thus, having each processing node initialize and test its own local memory, by executing a routine that tests and initializes memory.

Regarding Claims 2-4, 6, 7, 9-11, 13-15, 17-20, 22-25, Moyes discloses each processing node reports status, step 508, which occurs, for example, continuously during the memory initialization and test, periodically, or when memory initialization and testing are complete. After all processing nodes have completed memory initialization and test, the bootstrap processor continues with system boot and the other processing nodes halt, step 510.

Fig. 6 illustrates an exemplary status reporting mechanism 600, using periodic status reporting from the various processing nodes, where the boot strap processor can create a display for a computer screen depicting the current status, displays 602 [0:N]

depicting a percent completion of the memory initialization and testing process on each processing node and/or overall.

Regarding Claims 7, 8, 10, Moyes discloses error correction code (ECC) chip 404, which stores error correction codes that allow memory errors to be found and corrected. Additionally, DIMM 400 can have an SPD (serial presence detect) chip 406, which contains read only information specifying an operational range of DIMM 400 and other information similar to what one would find in a data sheet. For example, SPD chip 406 identifies memory storage capacity of DIMM 400, operating parameters such as minimum cycle times, CAS latency, Fig. 4.

Upon system initialization, each memory module must be initialized and tested. This can include verifying population of memory modules, verifying proper operation of the memory (no stuck bits), and initializing or clearing the memory to known values. Each memory module can be scrubbed on a periodic basis utilizing ECC to correct any memory errors.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Jacques H. Louis-Jacques can be reached on 571) 272-4150. The fax

phone number for the organization where this application or proceeding is assigned is
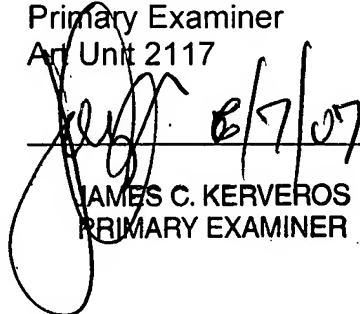
571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAMES C KERVEROS
Primary Examiner
Art Unit 2117

Date: 7 June 2007
Office Action: Non-Final Rejection

JAMES C. KERVEROS
PRIMARY EXAMINER

Tel: (571) 272-3824, Fax: (571) 273-3824
Email: james.kerveros@uspto.gov
U.S. Patent and Trademark Office
Alexandria, VA 22314